POWER OF ATTORNEY

Commissioner for Patents
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GLOBALFOUNDRIES Inc., hereby revokes any previous Powers of Attorney and appoints the following attorneys and/or agents in connection with the patent applications and patents identified in Appendix A, owned by GLOBALFOUNDRIES Inc., that are filed with the United States Patent and Trademark Office:

I hereby revoke any previous Powers of Attorney and appoint **the practitioners at Customer Number 90828,** as its attorney or agent for so long as they remain with such firm, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the U.S. Patent and Trademark Office in connection therewith, and to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

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Reg. No.: 33,491
Title: Global IP Portfolio Counsel

APPENDIX A

Dkt.No	GF Ref	App. Date	App. No.	Pat. Date	Pat. No.	Title	Inventors
6363-00100	TT4899	7/8/2003	10/614,970			System And Method Of Implementing Microcode Operations As Subroutines	Mitchell Alsup, Gregory W. Smaus
6363-00201	DE0200	11/1/2002	10/285,939			Response Reordering Mechanism	Joerg Winkler, Frank Barth, Larry Hewitt
6363-00300	TT5374	12/3/2003	10/726,902			Transitioning From Instruction Cache To Trace Cache On Label Boundaries	Mitchell Alsup, Gregory William Smaus
6363-00400	TT5526	12/5/2003	10/729,321			History File Coupled To Register File Write	Stephan G. Meier
6363-00500	TT5528	12/9/2003	10/730,800			Apparatus And Method For Multiple Pass Extended Precision Floating Point Multiplication	Debjit Das Sarma
6363-00600	TT5529	9/3/2003	10/653,754			Low Power Way-Predicted Cache	Stephan G. Meier, S. Craig Nelson, Gene W. Shen
6363-00700	TT5451	4/7/2004	10/819451			Transitioning From Instruction Cache To Trace Cache On Label Boundaries	Patrick N. Conway
6363-00701	TT5451DIV	5/12/2008	12/118,818			Transitioning From Instruction Cache To Trace Cache On Label Boundaries	Patrick N. Conway
6363-00800	DE0467	11/4/2003	10/701,108			Hardware/Software Split For A Networking Device	Ralf Flemming, Stephan Rosner, William Kern, Mathias Baer, William M. Johnson, Terry L. Cole
6363-00900	TT4918	5/16/2002	10/147,425			Wireless Computer System With Frame Mapping	Stephan Rosner, William F. Kern, Ralf Flemming, Stephen T. Novak
6363-01000	TT5581	7/5/2005	11/175,089			High Speed Hardware Divider	Teik-Chung Tan, Wing-Shek Wong
6363-01101	DE0450	7/26/2004	10/899,200			Fast Ciphering Key Search For Wlan Receivers	Ingo Kuehn, Uwe Eckhardt, Axel Wachtler, Falk Tischer
6363-01200	TT5807	2/6/2006	11/348,136			Method And Apparatus For Crosstalk Reduction	Shawn Searles, Gerald R. Talbot
6363-01300	TT5818	3/21/2006	11/385,329			Incrementally Adjustable For Skew And Duty Cycle Correction For Clock Signals Within A Clock Distribution Network	Shawn Searles, Donald Walters, Ravinder Rachala, Scott C. Johnson
6363-01401	DE0430	7/14/2005	11/181,236			Low-If Multiple Mode Digital Receiver Front End And Corresponding Method	Michael Schmidt, Eric Sachse, Menno Mennenga
6363-01500	TT5850	2/25/2005	11/066,873			Virtualization Of Real Mode Execution	Alexander C. Klaiber, Kevin J. McGrath, Hongwen Gao

Dkt No.	GF Ref	App. Date	App. No.	Pat. Date	Pat. No.	Title	Inventors
6363-01600	TT5851	2/25/2005	11/066,027			Limiting Guest Execution	Alexander C. Klaiber
6363-01700	H2171	5/2/2005	11/119,656			Use Of One Or More Cpu Cores In A Chip Multiprocessor As An Offload Engine	Jeffrey Dwork, Patrick N. Conway, Frederick D. Weber, Charles Moore, Mark D. Hummel, Michael T. Clark, Stephen C. Hale
6363-01800	H2173	4/4/2008	12/098,303			Shared Resources In A Chip Multiprocessor	William A. Hughes, Vydhyanathan Kalyanasundharam, Kiran K. Bondalapati, Philip E. Madrid, Stephen C. Ennis
6363-01901	DE0409	7/14/2005	11/181,152			Low-If Multiple Mode Transmitter Front End And Corresponding Method	Sascha Beyer, Wolfram Kluge, Michael Schmidt
6363-02000	TT5835	8/2/2005	11/195,186			Call Return Stack Way Prediction Repair	Gregory William Smaus, Michael Tuuk, Raghuram S. Tupuri
6363-02101	DE0524	4/15/2005	11/106,774			Event List Specification Based Radio Interface Control	Derek Golightly
6363-02201	DE0584	12/21/2005	11/316,506			Portable Wireless Data Storage Device	Joerg Borowski, George Minassian, Joe Tom
6363-02301	DE0443	5/25/2006	11/440,944			Dynamic Synchronizer Simulation	Mark Langer, Nathan Sheeley, Kay Hesse, Tracy Harton
6363-02400	TT5951	11/16/2005	11/281,303			Method And Mechanism To Deter Attacks On Microcode Patching	Preetham Raghuvanshi, Norman M. Hack
6363-02500	H2265	6/30/2006	11/478,741			Portable Computing Platform Including Wireless Communication Functionality	R. Stephen Polzin, Robert Ober
6363-02600	H2267	6/30/2006	11/478,739			Platform Security For A Portable Computer System Including Wireless Functionality	R. Stephen Polzin, Robert Ober
6363-02700	H2269	6/30/2006	11/478,737			A Portable Computer System Having Wireless Communication Functionality And Global Geographic Positioning Functionality	Robert Ober, William T. Edwards, R. Stephen Polzin
6363-02800	H2271	6/30/2006	11/478,695			Apparatus And Method For Wireless Network Parameter Logging And Reporting Within A Portable Device Having Wireless Communication Functionality	Robert Ober
6363-02900	TT5960	5/10/2006	11/432,706			Blocking Aggressive Neighbors In A Cache Subsystem	Kevin M. Lepak, Roger D. Isaac

Dkt No	GF Ref	App. Date	App. No.	Pat. Date	Pat. No.	Title	Inventors
6363-03000	TT5970	8/14/2006	11/503,700			System And Method For Limiting Processor Performance	Francisco L. Duran, W. Paul Montgomery, David F. Tobias
6363-03101	DE0677	7/11/2006	11/484,295			Sram Cells Including Self-Stabilizing Transistor Structures	Frank Wirbeleit and Martin Majer
6363-03200	TT6015	3/6/2006	11/368,785			System And Method For Asymmetric Control Of High Speed Bidirectional Signaling	Gerald R. Talbot, R. Stephen Polzin
6363-03300	H2311	3/1/2006	11/365,706			System And Method For Secure Data In A Memory	R. Stephen Polzin
6363-03400	H2318	2/28/2007	11/711,925			Branch Predictor Directed Prefetch	Marius Evers, Trivikram Krishnamurthy
6363-03500	H2321	2/13/2007	11/674,566			Redirect Recovery Cache	Gene W. Shen, Sean Lie
6363-03600	H2326	6/26/2007	11/768,417			Immediate And Displacement Extraction And Decode Mechanism	Sean Lie
6363-03700	H2331	4/18/2007	11/788,215			Token Based Power Control Mechanism	Stephan Meier, Marius Evers
6363-03800	H2332	7/10/2007	11/775,456			Method And Apparatus For Length Decoding And Identifying Boundaries Of Variable Length Instructions	Gene W. Shen, Sean Lie
6363-03900	H2356	1/10/2008	11/972,166			Processor Including Hybrid Redundancy For Logic Error Protection	Michael G. Butler, Nhon Quach
6363-04000	H2357	7/12/2007	11/776,986			Mechanism For Identifying The Source Of Performance Loss In A Microprocessor	Nhon Quach, Sean Lie
6363-04100	H2376	11/26/2007	11/944,878			Floating Point Bypass Retry	Gary Lauterbach
6363-04200	H2378	11/26/2007	11/944,864			Mechanism To Accelerate Removal Of Store Operations From A Queue	Gary Lauterbach
6363-04300	TT6072	8/23/2006	11/508,494			Method For Creating Critical Section Code Using A Software Wrapper For Proactive Synchronization Within A Computer System	Mitchell Alsup
6363-04400	H2401	12/13/2006	11/610,191			Command Packet Packing To Mitigate Crc Overhead	William A. Hughes, Chen-Ping Yang, Greggory D. Donley, Michael K. Fertig
6363-04500	TT6082	9/11/2006	11/518843			System For Controlling High-Speed Bidirectional Communication	Gerald R. Talbot
6363-04600	TT6100	11/13/2006	11/559,049			Filtering And Remapping Interrupts	Mark D. Hummel, Andrew W. Lueck, Andrew G. Kegel
6363-04700	TT6144	10/31/2006	11/590,286			Memory Controller Including A Dual-Mode	Gerald R. Talbot

Dkt No	GF Ref	App. Date	App. No.	Pat. Date.	Pat. No.	Title	Inventors
6363-04800	TT6145	10/31/2006	11/590,290			Memory System Including Asymmetric High-Speed Differential Memory Interconnect	Gerald R. Talbot
6363-04900	TT6052	8/9/2007	11/836,201			System And Method For Controlling Synchronous Functional Microprocessor Redundancy During Test And Method For Determining Results	Michael L. Choate, Arthur M. Ryan, Kevin E. Ayers, Ha Nguyen, and Douglas L. Terre
6363-05000	H2445	12/13/2006	11/610,219			Partial Crc Inseration In Data Packets For Early Forwarding	William A. Hughes, Chen-Ping Yang, Greggory D. Donley, Michael K. Fertig
6363-05100	TT6180	1/16/2007	11/623,626			Virtualization An Iommu	Mark D. Hummel, Andrew W. Lueck, Geoffrey S. Strongin, Mitchell Alsup, Michael Haertel
6363-05200	TT6181	1/16/2007	11/623,500			Dma Address Translation In An IOMMU	Mark D. Hummel, Geoffrey S. Strongin, Mitch Alsup, Michael Haertel, Andrew W. Lueck
6363-05300	TT6041	3/21/2007	11/688,017			Coherent Data Mover	Andrew R. Rawson
6363-05400	H2429	6/1/2007	11/756,984			Multiple Line Traffic Distribution	William A. Hughes, Chen-Ping Yang
6363-05500	H2438	7/19/2007	11/780,283			Speculative Memory Prefetch	Michael K Fertig, Patrick Conway, Kevin Lepak, Cissy Yuan
6363-05600	H2439	10/23/2007	11/877,311			Coherent Dram Prefetcher	Kevin Michael Lepak, Gregory William Smaus, William A. Hughes, Vydhyanathan Kalyanasundharam
6363-05700	H2447	7/26/2007	11/828,382			Method And Apparatus For Handling Excess Data During Memory Access	Greggory D. Donley
6363-05800	H2448	6/28/2007	11/769,970			Apparatus For Reducing Cache Latency While Preserving Cache Bandwidth In A Cache Subsystem Of A Processor	Greggory D. Donley, William A. Hughes
6363-05900	H2449	6/29/2007	11/771,299			Cache Memory Having Configurable Associativity	Greggory D. Donley
6363-06000	H2453	2/26/2008	12/037,595			Push For Sharing Instruction	John D. McCalpin, Patrick Conway
6363-06100	TT6051	8/31/2007	11/841,179			Method And Apparatus For Clock Cycle Stealing	Spencer M. Gold, Bill K.C. Kwan, Craig D. Eaton

Dkt No.	GF Ref.	App. Date	App. No.	Pat. Date	Pat. No.	Title	Inventors
6363-06201	DE0877	8/9/2007	11/891,165			Time Stamping Transactions To Validate Atomic Operations In Multiprocessor Systems	Padmaraj Singh, Todd Foster, Dennis Lastor
6363-06300	TT6167	8/16/2007	11/839,611			Level Shifter Circuit With Pre-Charge/Pre-Discharge	Calvin Watson
6363-06400	H2450	7/31/2007	11/831,119			Placing Virtual Machine Monitor (Vmm) Code In Guest Context To Speed Memory Mapped Input/Output Virtualization	Benjamin C. Serebrin
6363-06500	H2436	5/5/2008	12/115,355			Transient Transactional Cache	Michael Frank, David J. Leibs, Michael J. Haertel
6363-06600	TT6055	6/10/2008	12/136,458			Processor Test System Utilizing Functional Redundancy	Michael L. Choate, Mark D. Nicol, Heather L. Hanson, Michael J. Borsch, Arthur M. Ryan, Chandrakant Pandya
6363-06700	TT6146	7/30/2007	11/830,116			Shrink Test Mode To Identify Nth Order Speed Paths	Michael A. Comai, Philip E. Madrid
6363-06800	TT6149	8/22/2007	11/843,434			An Optimal Solution To Control Data Channels	Philip E. Madrid, Tahsin Askar
6363-06900	TT6310	12/17/2007	11/957,848			Uses Of Known Good Code For Implementing Processor Architectural Modifications	Garth D. Hillman, Geoffrey S. Strongin, Andrew R. Rawson, Gary H. Simpson, Ralf Findeisen
6363-07000	TT6248	3/31/2008	12/059,595			Cascode Driver With Gate Oxide Protection	Anil Kumar, Shawn Searles
6363-07100	TT6293	1/30/2008	12/022,446			Computer System Including A Main Processor And A Bond Security Coprocessor	Ralf Findeisen, Geoffrey S. Strongin, Andrew R. Rawson, Garth D. Hillman, Gary H. Simpson
6363-07200	TT6160	12/13/2007	11/955,976			Technique To Implement Clock-Gating	Umesh Chandra Chejara
6363-07300	TT6168	1/8/2008	11/970,782			Circuit Having Gate Oxide Protection For Low Voltage Fuse Reads And High Voltage Fuse Programming	Calvin Watson, Matthew Cooke
6363-07400	H2434	12/21/2007	11/962,778			Unified Processor Architecture For Processing General And Graphics Workload	Michael Frank
6363-07500	TT6164	1/29/2008	12/021,455			Test Access Mechanism For Multi-Core Processor Or Other Integrated Circuit	Grady L. Giles, Brian Hoang, Timothy J. Wood
6363-07600	TT6239	9/22/2008	12/235,155			Functional Block Level Thermal Control	Hanwoo Cho, Alexander Branover, Jonathan D. Hauke
6363-07700	TT6330	2/28/2008	12/039,278			Fast, Automatically Scaled Processor Time Stamp Counter	Benjamin C. Serebrin

Dkt No	GF Ref	App. Date	App. No.	Pat. Date.	Pat. No.	Title	Inventors
6363-07800	P0059	3/31/2008	12/059,543			A Low Overhead Soft Error Tolerant Flip Flop	Samuel D. Naffziger
6363-07900	TT6221	3/11/2008	12/045,916			Automatic Processor Overclocking	Spencer M. Gold, Alex Branover, Hanwoo Cho, and Sebastien Nussbaum
6363-08000	TT6349	3/11/2008	12/045,764			A Protocol For Transistioning In And Out Of Zero-Power State	Alexander Branover, Rajen S. Ramchandani
6363-08100	TT6285	8/26/2008	12/198,239			Hardware Based Multi-Dimensional Encryption	Andrew R. Rawson, Sr.
6363-08200	P0058	4/9/2008	12100052			Programmable Sample Clock For Empirical Setup Time Selection	Samuel D. Naffziger
6363-08301	DE0876	1/28/2008	12/011,515			Latency Coverage And Adoption To Multi-Processor Test Generator Template Creation	Padmaraj Singh, Todd Foster, Dennis Lastor
6363-08400	TT6370	12/18/2007	11/958,764			Mechanism For Profiling Program Software Running On A Processor	Anton Chernoff
6363-08500	TT6378	4/30/2008	12/112,611			Translation Data Prefetch In An IOMMU	Andrew G. Kegel, Mark D. Hummel, Erich S. Boleyn
6363-08600	H2559	2/4/2009	12/365,543			Processor Instructions For Improved Aes Encryption And Decryption	Michael Frank
6363-08700	H2545	12/5/2008	12/329,236			Method And Apparatus For Fast Decompression Of Block Compressed Data	Michael Frank
6363-08800	TT6460	8/27/2008	12/198,974			Hardware Monitoring And Decision Making For Transitioning In And Out Of Low-Power State	Alexander Branover, Frank Helms, Maurice Steinman
6363-08900	TT6461	12/12/2008	12/333,744			Enhanced Control Of Cpu Parking And Thread Rescheduling For Maximizing The Benefits Of Low-Power State	Alexander Branover, Maurice B. Steinman, Denis Rystsov
6363-09000	TT6462	10/20/2008	12/254,650			A Protocol For Power State Determination And Demotion	Alexander Branover, Frank P. Helms, John P. Petry, Maurice B. Steinman
6363-09100	P0066	11/11/2008	12/268,531			Method And Apparatus For Regulating Power Consumption	Samuel D. Naffziger, Sebastien J. Nussbaum
6363-09200	TT6475	2/20/2009	12/389,748			Method And System For Performing A Double Pass Nth Fail Bitmap Of A Device Memory	Debaleena Das
6363-09300	DE1217	7/28/2008	61/084,008			Advanced Synchronization Facility	Michael P. Hohmuth, David S. Christie, Stephan Diestelhorst

Dkt No	GE Ref	App. Date	App. No.	Pat. Date.	Pat. No.	Title	Inventors
6363-09400	TT6486	9/17/2008	12/212,370			Minimizing Memory Access Conflicts Of Process Communication Channels	Sebastian Pop, Jan Sjodin, Harsha Jagasia
6363-09500	TT6455	11/3/2008	12/263,902			System For Dynamic Program Profiling	Richard C. Gorton, Jr.
6363-09600	TT6458	10/10/2008	12/249,446			Register Reduction And Liveness Analysis Techniques For Program Code	David A. Kaplan
6363-09700	H2606	11/18/2008	12/272,946			Alternate Address Space To Permit Virtual Machine Monitor Access To Guest Virtual Address Space	Benjamin C. Serebrin, Michael J. Haertel
6363-09800	H2608	11/18/2008	12/272,955			Minivisory Entry Point In Virtual Machine Monitor Address Space	Benjamin C. Serebrin
6363-09900	H2613	11/18/2008	12/272,951			Execute-Only Memory And Mechanism Enabling Execution From Execute-Only Memory For Minivisor	Benjamin C. Serebrin
6363-10000	TT6514	12/18/2008	12/338,459			Optimization Of Application Power Consumption And Performance In An Integrated System On A Chip	Alexander Branover, Helmut W. Prengel, Anthony Asaro, Sebastian Nussbaum and Maurice B. Steinman
6363-10100	TT6512	1/15/2009	12/354,435			Application Partitioning Across A Virtualized Enviroment	Azeem S. Jiva
6363-10200	H2632	1/7/2009	12/349,810			Pseudo-Bandgap Voltage Reference Circuit	Emerson S. Fang, Tin Tin Wee, Sanjeev K. Maheshwari
6363-10300	TT0517	06/07/1995	08/482046			Information Flow Through Alternate Data Buses	Gephardt, Stewart, Wisor, Dutton, Belt
6363-10301	TT0517CNT	11/19/2004	10/993095			Information Flow Through Alternate Data Buses	Gephardt, Stewart, Wisor, Dutton, Belt
6363-10400	TT5312	09/30/2002	10/261643	06/13/2006	7062610	Method And Apparatus For Reducing Overhead In A Data Processing System	Conway
6363-10500	TT5357	05/09/2003	10/434692	02/19/2008	7334102	Apparatus And Method For Balanced Spinlock Support In NUMA Systems	Conway
6363-10600	TT5639	02/09/2005	11/054220			Data Processor Adapted For Efficient Digital Signal Processing And Method Thereof	Cole, Nichols, Johnson, Kutagulla
6363-10700	TT5650	07/08/2004	10/887069			Data Processor Having A Cache With Efficient Storage Of Predecode Information	Muthusamy, McMinn

Dkt.No	GF Ref	App. Date	App. No.	Pat. Date	Pat. No.	Title	Inventors
6363-10800	H0116	8/29/02	10/230775	4/21/09	7521304	Method For Forming Integrated Circuit	Huang, Richard J.; Bell, Scott A.; Dakshina-Murthy, Srikanteswara; Fisher, Philip A.; Nguyen, Richard C.; Tabery, Cyrus E.; You, Lu
6363-10801	H0116CNT	4/20/09	12/426812			Method For Forming Integrated Circuit	Huang, Richard J.; Bell, Scott A.; Dakshina-Murthy, Srikanteswara; Fisher, Philip A.; Nguyen, Richard C.; Tabery, Cyrus E.; You, Lu
6363-10900	H0963	1/14/03	10/341863			Shallow Trench Isolation For Strained Silicon Processes	Ngo, Mish-Van; Xiang, Qui; Besser, Paul R.; Paton, Eric N.; Lon, Ming-Ren
6363-11000	H0979	4/7/04	10/819441	2/28/06	7005302	Semiconductor On Insulator Substrate And Devices Formed Therefrom	Xiang, Qi
6363-11004	H0979DIV	2/24/06	11/361207	5/22/07	7221025	Semiconductor On Insulator Substrate And Devices Formed Therefrom	Xiang, Qi
6363-11100	H1721	12/5/03	10/729479	12/5/06	7144818	Semiconductor Substrate And Processes Therefor	Pelella, Mario M.; Chan, Simon S.
6363-11106	H1721DIV	7/12/05	11/179282	9/4/07	7265420	Semiconductor Substrate Layer Configured For Inducement Of Compressive Or Expansive Force	Pelella, Mario M.; Chan, Simon S.
6363-11200	H1718	1/12/04	10/755602	12/9/08	7462549	Shallow Trench Isolation Process And Structure With Minimized Strained Silicon Consumption	Xiang, Qi; Pan, James N.; Goo, Jung-Suk
6363-11207	H1718DIV	5/5/08	12/115473			Shallow Trench Isolation Process And Structure With Minimized Strained Silicon Consumption	Xiang, Qi; Pan, James N.; Goo, Jung-Suk
6363-11300	H0967	10/29/02	10/282559	3/9/04	6703648	Strained Silicon Pmos Having Silicon Germanium Source/Drain Extensions And Method For Its Fabrication	Xiang, Qi; Paton, Eric N.; Wang, Haihong
6363-11301	H0967DIV	12/17/03	10/738716	7/4/06	7071065	Strained Silicon Pmos Having Silicon Germanium Source/Drain Extensions And Method For Its Fabrication	Xiang, Qi; Paton, Eric N.; Wang, Haihong
6363-11400	H2180	4/4/05	11/098049	4/22/08	7361588	Etch Process For Cd Reduction Of Arc Material	Jones, Phillip L.; Chang, Mark S.; Bell, Scott A.

Dkt No	GF Ref	App. Date	App. No.	Pat. Date.	Pat. No.	Title	Inventors
6363-11500	H0962	3/14/03	10/389456	9/9/08	7422961	Method Of Forming Isolation Regions For Integrated Circuits	Wang, Haihong; Ngo, Minh-Van; Xiang, Qi; Besser, Paul R.; Paton, Eric N.; Lin, Ming-Ren
6363-11501	H0962DIV	9/5/08	12/205361			Method Of Forming Isolation Regions For Integrated Circuits	Wang, Haihong; Ngo, Minh-Van; Xiang, Qi; Besser, Paul R.; Paton, Eric N.; Lin, Ming-Ren